

	L #	Hits	Search Text	DBs
1	L1	13583	floating adj point	USPAT; US-PGPUB
2	L2	1105	pipelin\$3 near50 1	USPAT; US-PGPUB
3	L3	777	(exception fault trap\$4) near20 1	USPAT; US-PGPUB
4	L4	12071	insert\$3 near10 (command instruction)	USPAT; US-PGPUB
5	L5	3	3 near99 4	USPAT; US-PGPUB
6	L6	142	(exception fault trap\$4) near50 4	USPAT; US-PGPUB
7	L7	129670	(return\$3 roll\$3 unroll\$3 play\$3 replay\$3 (re adj execut\$3) reexecut\$3) near50 (state status)	USPAT; US-PGPUB
8	L8	438	(2 3 6) and 7	USPAT; US-PGPUB
9	L9	19000	floating.ab,ti.	USPAT; US-PGPUB
10	L11	278	2 and 3 not 10	USPAT; US-PGPUB
11	L10	49	8 and 9	USPAT; US-PGPUB
12	L12	57	8 and 11 not 10	USPAT; US-PGPUB
13	L15	11	3 and 6 not (10 12)	USPAT; US-PGPUB
14	L16	192	(floating adj point) near50 pipelin\$3	EPO; JPO; DERWENT; IBM_TDB
15	L17	108	(floating adj point) near20 (exception trap\$4 fault)	EPO; JPO; DERWENT; IBM_TDB
16	L18	60	(insert\$3 near10 (instruction command)) near50 (exception trap\$4 fault)	EPO; JPO; DERWENT; IBM_TDB
17	L19	125953	(return\$3 roll\$3 unroll\$3 play\$3 replay\$3 (re adj execut\$3) reexecut\$3 singl\$3) near50 (state status)	EPO; JPO; DERWENT; IBM_TDB
18	L21	22	16 and 17	EPO; JPO; DERWENT; IBM_TDB
19	L20	4	(16 17) and (18 19)	EPO; JPO; DERWENT; IBM_TDB

	Docum ent ID	U	Title	Current OR
1	US 20030 12641 9 A1	<input type="checkbox"/>	Exception masking in binary translation	712/244
2	US 20020 03271 8 A1	<input type="checkbox"/>	METHOD AND APPARATUS FOR MAINTAINING TRANSLATED ROUTINE STACK IN A BINARY TRANSLATION ENVIROMENT	709/107
3	US 65499 59 B1	<input type="checkbox"/>	Detecting modification to computer memory by a DMA device	710/22
4	US 65359 03 B2	<input type="checkbox"/>	Method and apparatus for maintaining translated routine stack in a binary translation environment	709/100
5	US 65022 37 B1	<input type="checkbox"/>	Method and apparatus for performing binary translation method and apparatus for performing binary translation	717/136
6	US 63973 79 B1	<input type="checkbox"/>	Recording in a program execution profile references to a memory-mapped active device	717/140
7	US 62267 89 B1	<input type="checkbox"/>	Method and apparatus for data flow analysis	717/138
8	US 61990 95 B1	<input type="checkbox"/>	System and method for achieving object method transparency in a multi-code execution environment	709/107
9	US 61345 73 A	<input type="checkbox"/>	Apparatus and method for absolute floating point register addressing	708/510
10	US 60918 97 A	<input type="checkbox"/>	Fast translation and execution of a computer program on a non-native architecture by use of background translator	717/138
11	US 60000 28 A	<input type="checkbox"/>	Means and apparatus for maintaining condition codes in an unevaluated state	712/226
12	US 59305 09 A	<input type="checkbox"/>	Method and apparatus for performing binary translation	717/159
13	US 59151 17 A	<input type="checkbox"/>	Computer architecture for the deferral of exceptions on speculative instructions	710/262
14	US 58420 17 A	<input type="checkbox"/>	Method and apparatus for forming a translation unit	717/158
15	US 58359 67 A	<input type="checkbox"/>	Adjusting prefetch size based on source of prefetch address	711/213
16	US 58359 51 A	<input type="checkbox"/>	Branch processing unit with target cache read prioritization protocol for handling multiple hits	711/145
17	US 58023 73 A	<input type="checkbox"/>	Method for providing a pipeline interpreter for a variable length instruction set	717/139
18	US 57782 11 A	<input type="checkbox"/>	Emulating a delayed exception on a digital computer having a corresponding precise exception mechanism	703/26
19	US 57404 16 A	<input type="checkbox"/>	Branch processing unit with a far target cache accessed by indirection from the target cache	712/238
20	US 57322 53 A	<input type="checkbox"/>	Branch processing unit with target cache storing history for predicted taken branches and history cache storing history for predicted not-taken branches	712/239
21	US 57322 43 A	<input type="checkbox"/>	Branch processing unit with target cache using low/high banking to support split prefetching	711/137
22	US 57064 91 A	<input type="checkbox"/>	Branch processing unit with a return stack including repair using pointers from different pipe stages	712/234

	Docum ent ID	U	Title	Current OR
23	US 56921 68 A	<input type="checkbox"/>	Prefetch buffer using flow control bit to identify changes of flow within the code stream	712/237
24	US 56529 00 A	<input type="checkbox"/>	Data processor having 2n bits width data bus for context switching function	709/100
25	US 55600 36 A	<input type="checkbox"/>	Data processing having incircuit emulation function	712/227
26	US 55487 36 A	<input type="checkbox"/>	Method and apparatus overcoming delay introduced by instruction interlocking in pipelined instruction execution	712/244
27	US 55028 27 A	<input type="checkbox"/>	Pipelined data processor for floating point and integer operation with exception handling	712/244
28	US 54817 34 A	<input type="checkbox"/>	Data processor having 2n bits width data bus for context switching function	712/225
29	US 54407 57 A	<input type="checkbox"/>	Data processor having multistage store buffer for processing exceptions	712/228

	Docum ent ID	U	Title	Current OR
1	US 20020 17432 3 A1	<input type="checkbox"/>	Floating point unit pipeline synchronized with processor pipeline	712/220
2	US 64185 28 B1	<input checked="" type="checkbox"/>	Floating point unit pipeline synchronized with processor pipeline	712/212
3	US 59699 75 A	<input checked="" type="checkbox"/>	Data processing apparatus registers	708/490
4	US 58812 63 A	<input checked="" type="checkbox"/>	Non-instruction base register addressing in a data processing apparatus	712/217
5	US 58812 59 A	<input checked="" type="checkbox"/>	Input operand size and hi/low word selection control in data processing systems	712/210
6	US 58812 57 A	<input checked="" type="checkbox"/>	Data processing system register control	712/200
7	US 58600 00 A	<input checked="" type="checkbox"/>	Floating point unit pipeline synchronized with processor pipeline	712/244
8	US 58124 39 A	<input checked="" type="checkbox"/>	Technique of incorporating floating point information into processor instructions	708/497
9	US 57846 02 A	<input checked="" type="checkbox"/>	Method and apparatus for digital signal processing for integrated circuit architecture	712/220
10	US 56665 37 A	<input checked="" type="checkbox"/>	Power down scheme for idle processor components	713/322
11	US 56492 08 A	<input checked="" type="checkbox"/>	Mechanism for handling non-maskable interrupt requests received from different sources	710/262
12	US 56383 06 A	<input checked="" type="checkbox"/>	Testing hooks for testing an integrated data processing system	702/119
13	US 56301 53 A	<input checked="" type="checkbox"/>	Integrated digital signal processor/general purpose CPU with shared internal memory	712/35
14	US 56258 28 A	<input checked="" type="checkbox"/>	Parallel operating CPU core and DSP module for executing sequence of vector DSP code instructions to generate decoded constellation points in QAM/TCM modem application	375/261
15	US 56131 49 A	<input checked="" type="checkbox"/>	Integrated data processing system utilizing successive approximation analog to digital conversion and PWM for parallel disconnect	712/36
16	US 56067 14 A	<input checked="" type="checkbox"/>	Integrated data processing system including CPU core and parallel, independently operating DSP module and having multiple operating modes	712/43
17	US 56030 17 A	<input checked="" type="checkbox"/>	Parallel integrated circuit having DSP module and CPU core operable for switching between two independent asynchronous clock sources while the system continues executing instructions	713/501
18	US 55926 77 A	<input checked="" type="checkbox"/>	Integrated data processing system including CPU core and parallel, independently operating DSP module	712/34
19	US 55903 57 A	<input checked="" type="checkbox"/>	Integrated CPU core and parallel, independently operating DSP module and time-critical core priority scheme	712/35
20	US 55902 94 A	<input checked="" type="checkbox"/>	Method and apparatus for retarting pipeline processing	712/244
21	US 55375 38 A	<input checked="" type="checkbox"/>	Debug mode for a superscalar RISC processor	714/38
22	US 55308 15 A	<input checked="" type="checkbox"/>	Apparatus and method for verifying the order and operation of a data processing device when asynchronous commands are held in a command queue	712/227

	Docum ent ID	U	Title	Current R
23	US 55198 79 A	<input checked="" type="checkbox"/>	Integrated circuit having CPU and DSP for executing vector lattice propagation instruction and updating values of vector Z in a single instruction cycle	712/35
24	US 54918 28 A	<input checked="" type="checkbox"/>	Integrated data processing system having CPU core and parallel independently operating DSP module utilizing successive approximation analog to digital and PWM for parallel disconnect	712/35
25	US 54871 73 A	<input checked="" type="checkbox"/>	DTMF detection in an integrated data processing system	712/35
26	US 53013 31 A	<input checked="" type="checkbox"/>	Interruption handling system	710/260
27	US 48796 76 A	<input type="checkbox"/>	Method and apparatus for precise floating point exceptions	708/505

	L #	Hits	Search Text	DBs
1	L1	13583	floating adj point	USPAT; US-PGPUB
2	L2	1105	pipelin\$3 near50 1	USPAT; US-PGPUB
3	L3	777	(exception fault trap\$4) near20 1	USPAT; US-PGPUB
4	L4	12071	insert\$3 near10 (command instruction)	USPAT; US-PGPUB
5	L5	3	3 near99 4	USPAT; US-PGPUB
6	L6	142	(exception fault trap\$4) near50 4	USPAT; US-PGPUB
7	L7	129670	(return\$3 roll\$3 unroll\$3 play\$3 replay\$3 (re adj execut\$3) reexecut\$3) near50 (state status)	USPAT; US-PGPUB
8	L8	438	(2 3 6) and 7	USPAT; US-PGPUB
9	L9	19000	floating.ab,ti.	USPAT; US-PGPUB
10	L11	278	2 and 3 not 10	USPAT; US-PGPUB
11	L10	49	8 and 9	USPAT; US-PGPUB
12	L12	57	8 and 11 not 10	USPAT; US-PGPUB
13	L15	11	3 and 6 not (10 12)	USPAT; US-PGPUB
14	L16	192	(floating adj point) near50 pipelin\$3	EPO; JPO; DERWENT; IBM_TDB
15	L17	108	(floating adj point) near20 (exception trap\$4 fault)	EPO; JPO; DERWENT; IBM_TDB
16	L18	60	(insert\$3 near10 (instruction command)) near50 (exception trap\$4 fault)	EPO; JPO; DERWENT; IBM_TDB
17	L19	125953	(return\$3 roll\$3 unroll\$3 play\$3 replay\$3 (re adj execut\$3) reexecut\$3 singl\$3) near50 (state status)	EPO; JPO; DERWENT; IBM_TDB
18	L21	22	16 and 17	EPO; JPO; DERWENT; IBM_TDB
19	L20	4	(16 17) and (18 19)	EPO; JPO; DERWENT; IBM_TDB
20	L22	0	(2 3) and (6 7) and 9 not (10 12 15)	USPAT; US-PGPUB
21	L24	0	9 and (precise\$3 and exception).ab,ti.	EPO; JPO; DERWENT; IBM_TDB
22	L23	11	9 and (precise\$3 and exception).ab,ti.	USPAT; US-PGPUB
23	L25	537	(translat\$3 target) near50 1	USPAT; US-PGPUB
24	L27	29	3 near99 25	USPAT; US-PGPUB
25	L28	27	(exception fault trap\$4) near10 precise\$3 near99 2	USPAT; US-PGPUB

	Docum ent ID	U	Title	Current OR
1	US 20020 17432 3 A1	<input type="checkbox"/>	Floating point unit pipeline synchronized with processor pipeline	712/220
2	US 64185 28 B1	<input checked="" type="checkbox"/>	Floating point unit pipeline synchronized with processor pipeline	712/212
3	US 60214 88 A	<input checked="" type="checkbox"/>	Data processing system having an apparatus for tracking a status of an out-of-order operation and method thereof	712/228
4	US 59665 30 A	<input checked="" type="checkbox"/>	Structure and method for instruction boundary machine state restoration	712/244
5	US 58600 00 A	<input checked="" type="checkbox"/>	Floating point unit pipeline synchronized with processor pipeline	712/244
6	US 58124 39 A	<input checked="" type="checkbox"/>	Technique of incorporating floating point information into processor instructions.	708/497
7	US 56734 26 A	<input checked="" type="checkbox"/>	Processor structure and method for tracking floating-point exceptions	712/244
8	US 56491 36 A	<input checked="" type="checkbox"/>	Processor structure and method for maintaining and restoring precise state at any instruction boundary	712/244
9	US 55465 54 A	<input checked="" type="checkbox"/>	Apparatus for dynamic register management in a floating point unit	711/203
10	US 55375 38 A	<input checked="" type="checkbox"/>	Debug mode for a superscalar RISC processor	714/38
11	US 48796 76 A	<input type="checkbox"/>	Method and apparatus for precise floating point exceptions	708/505

	L #	Hits	Search Text	DBs
1	L1	13583	floating adj point	USPAT; US-PGPUB
2	L2	1105	pipelin\$3 near50 1	USPAT; US-PGPUB
3	L3	777	(exception fault trap\$4) near20 1	USPAT; US-PGPUB
4	L4	12071	insert\$3 near10 (command instruction)	USPAT; US-PGPUB
5	L5	3	3 near99 4	USPAT; US-PGPUB
6	L6	142	(exception fault trap\$4) near50 4	USPAT; US-PGPUB
7	L7	129670	(return\$3 roll\$3 unroll\$3 play\$3 replay\$3 (re adj execut\$3) reexecut\$3) near50 (state status)	USPAT; US-PGPUB
8	L8	438	(2 3 6) and 7	USPAT; US-PGPUB
9	L9	19000	floating.ab,ti.	USPAT; US-PGPUB
10	L11	278	2 and 3 not 10	USPAT; US-PGPUB
11	L10	49	8 and 9	USPAT; US-PGPUB
12	L12	57	8 and 11 not 10	USPAT; US-PGPUB
13	L15	11	3 and 6 not (10 12)	USPAT; US-PGPUB
14	L16	192	(floating adj point) near50 pipelin\$3	EPO; JPO; DERWENT; IBM_TDB
15	L17	108	(floating adj point) near20 (exception trap\$4 fault)	EPO; JPO; DERWENT; IBM_TDB
16	L18	60	(insert\$3 near10 (instruction command)) near50 (exception trap\$4 fault)	EPO; JPO; DERWENT; IBM_TDB
17	L19	125953	(return\$3 roll\$3 unroll\$3 play\$3 replay\$3 (re adj execut\$3) reexecut\$3 singl\$3) near50 (state status)	EPO; JPO; DERWENT; IBM_TDB
18	L21	22	16 and 17	EPO; JPO; DERWENT; IBM_TDB
19	L20	4	(16 17) and (18 19)	EPO; JPO; DERWENT; IBM_TDB
20	L22	0	(2 3) and (6 7) and 9 not (10 12 15)	USPAT; US-PGPUB
21	L24	0	9 and (precise\$3 and exception).ab,ti.	EPO; JPO; DERWENT; IBM_TDB
22	L23	11	9 and (precise\$3 and exception).ab,ti.	USPAT; US-PGPUB



	Docum ent ID	U	Title	Current OR
1	US 20030 08435 3 A1	<input type="checkbox"/>	System and method for predictive power ramping	713/300
2	US 20020 01690 3 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
3	US 65780 59 B1	<input checked="" type="checkbox"/>	Methods and apparatus for controlling exponent range in floating-point calculations	708/496
4	US 64906 07 B1	<input checked="" type="checkbox"/>	Shared FP and SIMD 3D multiplier	708/620
5	US 63706 39 B1	<input checked="" type="checkbox"/>	Processor architecture having two or more floating-point status fields	712/222
6	US 63321 86 B1	<input checked="" type="checkbox"/>	Vector register addressing	711/217
7	US 62826 34 B1	<input checked="" type="checkbox"/>	Apparatus and method for processing data having a mixed vector/scalar register file	712/210
8	US 62826 30 B1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
9	US 62232 78 B1	<input checked="" type="checkbox"/>	Method and apparatus for floating point (FP) status word handling in an out-of-order (OOO) Processor Pipeline	712/227
10	US 62125 39 B1	<input checked="" type="checkbox"/>	Methods and apparatus for handling and storing bi-endian words in a floating-point processor	708/495
11	US 61890 94 B1	<input checked="" type="checkbox"/>	Recirculating register file	712/222
12	US 61516 69 A	<input checked="" type="checkbox"/>	Methods and apparatus for efficient control of floating-point status register	712/222
13	US 61450 49 A	<input checked="" type="checkbox"/>	Method and apparatus for providing fast switching between floating point and multimedia instructions using any combination of a first register file set and a second register file set	710/267
14	US 60761 55 A	<input checked="" type="checkbox"/>	Shared register architecture for a dual-instruction-set CPU to facilitate data exchange between the instruction sets	712/225
15	US 60493 43 A	<input checked="" type="checkbox"/>	Graphics processing unit and graphics processing system	345/501
16	US 60386 53 A	<input checked="" type="checkbox"/>	High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
17	US 59665 30 A	<input checked="" type="checkbox"/>	Structure and method for instruction boundary machine state restoration	712/244
18	US 58840 62 A	<input checked="" type="checkbox"/>	Microprocessor with pipeline status integrity logic for handling multiple stage writeback exceptions	712/218
19	US 58570 89 A	<input checked="" type="checkbox"/>	Floating point stack and exchange instruction	712/222
20	US 58322 92 A	<input checked="" type="checkbox"/>	High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
21	US 58225 79 A	<input checked="" type="checkbox"/>	Microprocessor with dynamically controllable microcontroller condition selection	712/245
22	US 58093 20 A	<input checked="" type="checkbox"/>	High-performance multi-processor having floating point unit	712/34

	Docum ent ID	U	Title	Current OR
23	US 58059 18 A	<input checked="" type="checkbox"/>	Dual-instruction-set CPU having shared register for storing data before switching to the alternate instruction set	712/43
24	US 57817 90 A	<input checked="" type="checkbox"/>	Method and apparatus for performing floating point to integer transfers and vice versa	712/23
25	US 56969 55 A	<input checked="" type="checkbox"/>	Floating point stack and exchange instruction	712/222
26	US 56850 09 A	<input checked="" type="checkbox"/>	Shared floating-point registers and register port-pairing in a dual-architecture CPU	712/23
27	US 56734 26 A	<input checked="" type="checkbox"/>	Processor structure and method for tracking floating-point exceptions	712/244
28	US 56689 84 A	<input checked="" type="checkbox"/>	Variable stage load path and method of operation	712/222
29	US 56491 36 A	<input checked="" type="checkbox"/>	Processor structure and method for maintaining and restoring precise state at any instruction boundary	712/244
30	US 56066 96 A	<input checked="" type="checkbox"/>	Exception handling method and apparatus for a microkernel data processing system	709/108
31	US 55838 05 A	<input checked="" type="checkbox"/>	Floating-point processor having post-writeback spill stage	708/495
32	US 55600 32 A	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
33	US 55465 54 A	<input checked="" type="checkbox"/>	Apparatus for dynamic register management in a floating point unit	711/203
34	US 55375 38 A	<input checked="" type="checkbox"/>	Debug mode for a superscalar RISC processor	714/38
35	US 55049 25 A	<input checked="" type="checkbox"/>	Apparatus and method for implementing interrupts in pipelined processors	712/244
36	US 55028 27 A	<input checked="" type="checkbox"/>	Pipelined data processor for floating point and integer operation with exception handling	712/244
37	US 54817 19 A	<input checked="" type="checkbox"/>	Exception handling method and apparatus for a microkernel data processing system	709/108
38	US 54816 93 A	<input checked="" type="checkbox"/>	Shared register architecture for a dual-instruction-set CPU	712/225
39	US 54209 89 A	<input checked="" type="checkbox"/>	Coprocessor interface supporting I/O or memory mapped communications	710/110
40	US 54189 16 A	<input checked="" type="checkbox"/>	Central processing unit checkpoint retry for store-in and store-through cache systems	712/228
41	US 51558 43 A	<input checked="" type="checkbox"/>	Error transition mode for multi-processor system	714/5
42	US 51538 48 A	<input checked="" type="checkbox"/>	Floating point processor with internal free-running clock	708/503
43	US 50518 85 A	<input checked="" type="checkbox"/>	Data processing system for concurrent dispatch of instructions to multiple functional units	712/215
44	US 50420 00 A	<input checked="" type="checkbox"/>	Integral transform method	708/404
45	US 48796 76 A	<input checked="" type="checkbox"/>	Method and apparatus for precise floating point exceptions	708/505

	Docum ent ID	U	Title	Current OR
46	US 48051 28 A	<input checked="" type="checkbox"/>	Format conversion system	708/204
47	US 47632 94 A	<input checked="" type="checkbox"/>	Method and apparatus for floating point operations	708/510
48	US 47362 91 A	<input checked="" type="checkbox"/>	General-purpose array processor	712/11
49	US 38724 42 A	<input type="checkbox"/>	SYSTEM FOR CONVERSION BETWEEN CODED BYTE AND FLOATING POINT FORMAT	708/204

	Docum ent ID	U	Title	Current OR
1	US 20030 13572 2 A1	<input type="checkbox"/>	Speculative load instructions with retry	712/235
2	US 20030 06147 0 A1	<input checked="" type="checkbox"/>	Power consumption reduction mechanism for pipeline stalls	712/219
3	US 20030 06146 7 A1	<input checked="" type="checkbox"/>	Scoreboarding mechanism in a pipeline that includes replays and redirects	712/217
4	US 20030 06146 5 A1	<input checked="" type="checkbox"/>	Issue and retirement mechanism in processor having different pipeline lengths	712/214
5	US 20030 00964 8 A1	<input checked="" type="checkbox"/>	Apparatus for supporting a logically partitioned computer system	711/202
6	US 64991 23 B1	<input checked="" type="checkbox"/>	Method and apparatus for debugging an integrated circuit	714/724
7	US 64386 71 B1	<input checked="" type="checkbox"/>	Generating partition corresponding real address in partitioned mode supporting system	711/173
8	US 63112 61 B1	<input checked="" type="checkbox"/>	Apparatus and method for improving superscalar processors	712/23
9	US 63049 63 B1	<input checked="" type="checkbox"/>	Handling exceptions occurring during processing of vector instructions	712/244
10	US 62471 13 B1	<input checked="" type="checkbox"/>	Coprocessor opcode division by data type	712/200
11	US 62405 08 B1	<input checked="" type="checkbox"/>	Decode and execution synchronized pipeline processing using decode generated memory read queue with stop entry to allow execution generated memory read	712/219
12	US 62126 29 B1	<input checked="" type="checkbox"/>	Method and apparatus for executing string instructions	712/241
13	US 62055 60 B1	<input checked="" type="checkbox"/>	Debug system allowing programmable selection of alternate debug mechanisms such as debug handler, SMI, or JTAG	714/34
14	US 61700 01 B1	<input checked="" type="checkbox"/>	System for transferring format data from format register to memory wherein format data indicating the distribution of single or double precision data type in the register bank	708/495
15	US 61382 30 A	<input checked="" type="checkbox"/>	Processor with multiple execution pipelines using pipe stage state information to control independent movement of instructions between pipe stages of an execution pipeline	712/216
16	US 61120 19 A	<input checked="" type="checkbox"/>	Distributed instruction queue	712/214
17	US 60732 31 A	<input checked="" type="checkbox"/>	Pipelined processor with microcontrol of register translation hardware	712/218
18	US 60214 86 A	<input checked="" type="checkbox"/>	Continued processing of out-of-order non-architectural operations upon exceptions until flushing by architectural operations exceptions to avoid resume deadlock	712/218
19	US 58388 97 A	<input checked="" type="checkbox"/>	Debugging a processor using data output during idle bus cycles	714/30
20	US 58359 67 A	<input checked="" type="checkbox"/>	Adjusting prefetch size based on source of prefetch address	711/213
21	US 58359 51 A	<input checked="" type="checkbox"/>	Branch processing unit with target cache read prioritization protocol for handling multiple hits	711/145

	Docum ent ID	U	Title	Current OR
22	US 58095 52 A	<input checked="" type="checkbox"/>	Data processing system, memory access device and method including selecting the number of pipeline stages based on pipeline conditions	711/169
23	US 57846 36 A	<input checked="" type="checkbox"/>	Reconfigurable computer architecture for use in signal processing applications	712/37
24	US 57845 89 A	<input checked="" type="checkbox"/>	Distributed free register tracking for register renaming using an availability tracking register associated with each stage of an execution pipeline	712/217
25	US 57817 53 A	<input checked="" type="checkbox"/>	Semi-autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for speculative and out-of-order execution of complex instructions	712/218
26	US 57685 75 A	<input checked="" type="checkbox"/>	Semi-Autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for sepculative and out-of-order execution of complex instructions	712/228
27	US 57649 38 A	<input checked="" type="checkbox"/>	Resynchronization of a superscalar processor	712/200
28	US 57581 12 A	<input checked="" type="checkbox"/>	Pipeline processor with enhanced method and apparatus for restoring register-renaming information in the event of a branch misprediction	712/217
29	US 57519 85 A	<input checked="" type="checkbox"/>	Processor structure and method for tracking instruction status to maintain precise state	712/218
30	US 57404 16 A	<input checked="" type="checkbox"/>	Branch processing unit with a far target cache accessed by indirection from the target cache	712/238
31	US 57322 53 A	<input checked="" type="checkbox"/>	Branch processing unit with target cache storing history for predicted taken branches and history cache storing history for predicted not-taken branches	712/239
32	US 57322 43 A	<input checked="" type="checkbox"/>	Branch processing unit with target cache using low/high banking to support split prefetching	711/137
33	US 57064 91 A	<input checked="" type="checkbox"/>	Branch processing unit with a return stack including repair using pointers from different pipe stages	712/234
34	US 56921 68 A	<input checked="" type="checkbox"/>	Prefetch buffer using flow control bit to identify changes of flow within the code stream	712/237
35	US 56734 08 A	<input checked="" type="checkbox"/>	Processor structure and method for renamable trap-stack	712/216
36	US 56597 21 A	<input checked="" type="checkbox"/>	Processor structure and method for checkpointing instructions to maintain precise state	712/228
37	US 56551 15 A	<input checked="" type="checkbox"/>	Processor structure and method for watchpoint of plural simultaneous unresolved branch evaluation	712/239
38	US 56511 24 A	<input checked="" type="checkbox"/>	Processor structure and method for aggressively scheduling long latency instructions including load/store instructions while maintaining precise state	712/215
39	US 56492 25 A	<input checked="" type="checkbox"/>	Resynchronization of a superscalar processor	712/23
40	US 56447 42 A	<input checked="" type="checkbox"/>	Processor structure and method for a time-out checkpoint	712/244
41	US 56301 49 A	<input checked="" type="checkbox"/>	Pipelined processor with register renaming hardware to accommodate multiple size registers	712/217
42	US 56110 71 A	<input checked="" type="checkbox"/>	Split replacement cycles for sectorred cache lines in a 64-bit microprocessor interfaced to a 32-bit bus architecture	711/133

	Docum ent ID	U	Title	Current OR
43	US 55967 33 A	<input checked="" type="checkbox"/>	System for exception recovery using a conditional substitution instruction which inserts a replacement result in the destination of the excepting instruction	712/244
44	US 55967 31 A	<input checked="" type="checkbox"/>	Single clock bus transfers during burst and non-burst cycles	710/305
45	US 55903 59 A	<input checked="" type="checkbox"/>	Method and apparatus for generating a status word in a pipelined processor	712/32
46	US 55902 94 A	<input checked="" type="checkbox"/>	Method and apparatus for retarding pipeline processing	712/244
47	US 55600 36 A	<input checked="" type="checkbox"/>	Data processing having incircuit emulation function	712/227
48	US 55465 51 A	<input checked="" type="checkbox"/>	Method and circuitry for saving and restoring status information in a pipelined computer	707/102
49	US 55443 42 A	<input checked="" type="checkbox"/>	System and method for prefetching information in a processing system	711/119
50	US 55420 58 A	<input checked="" type="checkbox"/>	Pipelined computer with operand context queue to simplify context-dependent execution flow	713/502
51	US 54887 30 A	<input checked="" type="checkbox"/>	Register conflict scoreboard in pipelined computer using pipelined reference counts	712/41
52	US 54816 89 A	<input checked="" type="checkbox"/>	Conversion of internal processor register commands to I/O space addresses	711/202
53	US 54715 91 A	<input checked="" type="checkbox"/>	Combined write-operand queue and read-after-write dependency scoreboard	712/217
54	US 54505 55 A	<input checked="" type="checkbox"/>	Register logging in pipelined computer using register log queue of register content changes and base queue of register log queue pointers for respective instructions	712/228
55	US 53945 29 A	<input checked="" type="checkbox"/>	Branch prediction unit for high-performance processor	712/240
56	US 53332 96 A	<input checked="" type="checkbox"/>	Combined queue for invalidates and return data in multiprocessor system	711/171
57	US 53177 20 A	<input type="checkbox"/>	Processor system with writeback cache using writeback and non writeback transactions stored in separate queues	711/143

	Docum ent ID	U	Title	Current OR
1	US 20030 12641 9 A1	<input type="checkbox"/>	Exception masking in binary translation	712/244
2	US 64808 18 B1	<input checked="" type="checkbox"/>	Debugging techniques in a multithreaded environment	703/26
3	US 62956 01 B1	<input checked="" type="checkbox"/>	System and method using partial trap barrier instruction to provide trap barrier class-based selective stall of instruction processing pipeline	712/244
4	US 61158 11 A	<input checked="" type="checkbox"/>	Digital data process system including efficient arrangement to support branching within trap shadows	712/244
5	US 60095 15 A	<input checked="" type="checkbox"/>	Digital data processing system including efficient arrangement to support branching within trap shadows	712/244
6	US 59616 30 A	<input checked="" type="checkbox"/>	Method and apparatus for handling dynamic structural hazards and exceptions by using post-ready latency	712/200
7	US 58871 60 A	<input checked="" type="checkbox"/>	Method and apparatus for communicating integer and floating point data over a shared data path in a single instruction pipeline processor	712/222
8	US 58092 71 A	<input checked="" type="checkbox"/>	Method and apparatus for changing flow of control in a processor	712/208
9	US 57297 28 A	<input checked="" type="checkbox"/>	Method and apparatus for predicting, clearing and redirecting unpredicted changes in instruction flow in a microprocessor	712/234
10	US 56873 38 A	<input checked="" type="checkbox"/>	Method and apparatus for maintaining a macro instruction for refetching in a pipelined processor	712/205
11	US 53013 12 A	<input type="checkbox"/>	Method and system for utilizing benign fault occurrence to measure interrupt-blocking times	714/32

	L #	Hits	Search Text	DBs
1	L1	13583	floating adj point	USPAT; US-PGPUB
2	L2	1105	pipelin\$3 near50 1	USPAT; US-PGPUB
3	L3	777	(exception fault trap\$4) near20 1	USPAT; US-PGPUB
4	L4	12071	insert\$3 near10 (command instruction)	USPAT; US-PGPUB
5	L5	3	3 near99 4	USPAT; US-PGPUB
6	L6	142	(exception fault trap\$4) near50 4	USPAT; US-PGPUB
7	L7	129670	(return\$3 roll\$3 unroll\$3 play\$3 replay\$3 (re adj execut\$3) reexecut\$3) near50 (state status)	USPAT; US-PGPUB
8	L8	438	(2 3 6) and 7	USPAT; US-PGPUB
9	L9	19000	floating.ab,ti.	USPAT; US-PGPUB
10	L11	278	2 and 3 not 10	USPAT; US-PGPUB
11	L10	49	8 and 9	USPAT; US-PGPUB
12	L12	57	8 and 11 not 10	USPAT; US-PGPUB
13	L15	11	3 and 6 not (10 12)	USPAT; US-PGPUB



	Docum ent ID	U	Title	Current OR
1	JP 05233 229 A	<input type="checkbox"/>	INFORMATION PROCESSOR AND INFORMATION PROCESSING METHOD	
2	JP 02010 427 A	<input checked="" type="checkbox"/>	METHOD AND DEVICE FOR PRECISE FLOATING POINT EXCEPTION	
3	EP 77957 7 A2	<input checked="" type="checkbox"/>	Microprocessor pipe control and register translation	
4	EP 68455 2 A1	<input checked="" type="checkbox"/>	PROCESSOR SYSTEM AND DEBUG MODE ACCOMPLISHMENT METHOD.	
5	EP 64908 6 A1	<input checked="" type="checkbox"/>	Microprocessor with speculative execution.	
6	EP 64908 5 A1	<input checked="" type="checkbox"/>	Microprocessor pipe control and register translation.	
7	EP 30689 1 A2	<input checked="" type="checkbox"/>	Pipelined slave protocol for high performance CPU-FPU cluster.	
8	NB940 6211	<input checked="" type="checkbox"/>	Interface to a Floating Point Processor	
9	NN911 117	<input checked="" type="checkbox"/>	Efficient Operating System Support for Floating Point Trapping on a Heavily Pipelined Hardware Architecture.	
10	US 62090 83 B	<input checked="" type="checkbox"/>	Processor operating method for computer systems, involves delaying issue of next instruction until floating point unit clears preceding instruction, in normal operational mode	
11	JP 11327 903 A	<input checked="" type="checkbox"/>	Operation execution controller of floating point unit in computer system - checks corresponding system register mark, when event requiring milli code emulation is detected dynamically, based on which completion or restriction of operation is judged	
12	US 58840 62 A	<input checked="" type="checkbox"/>	Superscalar pipelined microprocessor integrated circuit in data processing system	
13	US 58840 57 A	<input checked="" type="checkbox"/>	System for temporal realignment of floating point pipeline to integer pipeline for emulation of load operate architecture on load/store processor	
14	US 57297 29 A	<input checked="" type="checkbox"/>	Fast trap ordering for pipelined multiscalar microprocessor - includes early and late trap units in execution units with mask generation logic coupling trap units to registers	
15	US 55599 77 A	<input checked="" type="checkbox"/>	Floating point instruction pair in pipelined processor - involves stalling following floating point instruction in execution stage if immediate floating point instruction pair is capable of raising exception	
16	US 55028 27 A	<input checked="" type="checkbox"/>	Pipelined data processor for floating point and integer operation with exception handling - has control unit which, when exception signal is asserted by execution unit, writes new data to register, receives exception, and activates exception processing handler	
17	EP 68455 2 B	<input checked="" type="checkbox"/>	Processor system with debug mode accomplishment method - has interrupt unit switching between normal and debug modes where command not executed until judged whether exception produced	
18	US 54169 12 A	<input checked="" type="checkbox"/>	Pipeline parallel processing units executions exception handling - receiving first floating point instruction from control memory and storing it in first and second latching devices	
19	EP 64908 6 A	<input checked="" type="checkbox"/>	Pipelined microprocessor with speculative instruction execution - issues speculation instructions e.g branches and floating point instructions and checks processor state to enable execution pipeline repair for branch mis-prediction or floating point exception	
20	US 53073 01 A	<input checked="" type="checkbox"/>	Safe instruction recognition for pipelined floating-point processor - analyses exponents of each operand, which are declared safe to ensure against floating-point processor overflow and underflow exceptions for add, subtract, multiply and divide operations	

	Docum ent ID	U	Title	Current OR
21	EP 58825 2 A	<input checked="" type="checkbox"/>	Instruction processing appts. for pipelined processors - has floating point register with several addressable storage elements for operand data, two address receiver circuits, register output, instruction execution unit with exception circuit, and shift register	
22	EP 30689 1 A	<input type="checkbox"/>	Pipelined slave protocol for high performance CPU-fpu cluster - uses storage on CPU for status information related to floating point co-processor and uses overlapped execution	

	Docum ent ID	U	Title	Current OR
1	JP 20011 47809 A	<input type="checkbox"/>	COMPUTER SYSTEM AND METHOD FOR DECIDING EXISTENCE OF FPU IN COMPUTER SYSTEM	
2	EP 90366 4 A2	<input checked="" type="checkbox"/>	Floating-point processor with operand-format precision greater than execution precision	
3	US 59616 30 A	<input checked="" type="checkbox"/>	Instruction scheduling method for execution in digital processor	
4	EP 28711 5 A	<input type="checkbox"/>	Floating point arithmetic co-processor control system - divides functions of co-processor into separate streams for pipeline control and stores instructions in FIFO	